WHAT IS CLAIMED IS:

1. An adder circuit for determining the sum of two operands, comprising:

a set of PGK circuits configured to generate propagate, generate, and kill bits corresponding to at least a portion of the first and second operands;

at least one tier of group circuits configured to receive the propagate, generate, and kill bits from a plurality of the PGK circuits and to produce, in response thereto, a set of group propagate, generate, and kill values;

a carry generation circuit configured to receive a carry-in bit and the outputs of at least one of the group circuits and further configured to generate a carry-out bit representing the carry-out of the corresponding group; and

a select circuit configured to select between a first sum and a second sum responsive to the carry-out bit.

2. The adder circuit of claim 1, wherein each generate bit is the logical AND of its corresponding bits in the first and second operand, each propagate bit is the EXOR of its corresponding bits in the first and second operands, and each kill bits is the logical NOR of its corresponding bits in the first and second operands.

3. The adder circuit of claim 1, wherein at least one of the PGK circuits, group circuits, and carry circuits includes at least one CMOS transmission gate.

4. The adder circuit of claim 3, wherein the PGK circuits, group circuits, and carry circuits are implemented primarily with CMOS transmission gates.

5. The adder circuit of claim 1, wherein the PGK circuits further generate the logical complements of the propagate, generate, and kill bits substantially simultaneously with the generation of the propagate, generate, and kill bits.

6. The adder circuit of claim 5, wherein the group circuits further generate the logical complements of the group propagate, generate, and kill values.

7. The adder circuit of claim 6, wherein the PGK and group circuits are implemented primarily with CMOS transmission gates.

8. The adder circuit of claim 1, wherein the at least one tier of group circuits includes a first tier of group circuits configured to receive the output of the PGK circuits and to generate an intermediate set of group propagate, generate, and kill values, and a second tier of at least one group circuit configured to receive the intermediate set of group propagate, generate, and kill values and to produce a final group propagate, generate, and kill values.

9. The adder circuit of claim 8, wherein the intermediate group of propagate, generate, and kill values each corresponds to a group of four adjacent bits and further wherein the final group of propagate, generate, and kill values correspond to a group of 16 adjacent bits.

10. The adder circuit of claim 1, wherein the carry-out bits generated by each of the carry generation circuits is used to select between a first sum and a second sum.

11. A microprocessor including and adder circuit for determining the sum of two operands, the adder comprising:

a set of PGK circuits configured to generate propagate, generate, and kill bits corresponding to at least a portion of the first and second operands;

at least one tier of group circuits configured to receive the propagate, generate, and kill bits from a plurality of the PGK circuits and to produce, in response thereto, a set of group propagate, generate, and kill values;

a carry generation circuit configured to receive a carry-in bit and the outputs of at least one of the group circuits and further configured to generate a carry-out bit representing the carry-out of the corresponding group; and

a select circuit configured to select between a first sum and a second sum responsive to the carry-out bit.

12. The microprocessor of claim 11, wherein each generate bit is the logical AND of its corresponding bits in the first and second operand, each propagate bit is the EXOR of its corresponding bits in the first and second operands, and each kill bits is the logical NOR of its corresponding bits in the first and second operands.

13. The microprocessor of claim 11, wherein at least one of the PGK circuits, group circuits, and carry circuits includes at least one CMOS transmission gate.

14. The microprocessor of claim 13, wherein the PGK circuits, group circuits, and carry circuits are implemented primarily with CMOS transmission gates.

15. The microprocessor of claim 11, wherein the PGK circuits further generate the logical complements of the propagate, generate, and kill bits substantially simultaneously with the generation of the propagate, generate, and kill bits.

16. The microprocessor of claim 15, wherein the group circuits further generate the logical complements of the group propagate, generate, and kill values substantially simultaneously with the generation of the group propagate, generate, and kill values.

17. The microprocessor of claim 16, wherein the PGK and group circuits are implemented primarily with CMOS transmission gates.

18. The microprocessor of claim 11, wherein the at least one tier of group circuits includes a first tier of group circuits configured to receive the output of the PGK circuits and to generate an intermediate set of group propagate, generate, and kill values, and a second tier of at least one group circuit configured to receive the intermediate set of group propagate, generate, and kill values and to produce a final group propagate, generate, and kill values.

19. The microprocessor of claim 18, wherein the intermediate group of propagate, generate, and kill values each corresponds to a group of four adjacent bits and further wherein the final group of propagate, generate, and kill values correspond to a group of 16 adjacent bits.

20. The microprocessor of claim 11, wherein the carry-out bits generated by each of the carry generation circuits is used to select between a first sum and a second sum.